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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,792	12/28/2000	Zhong-Ning (George) Cai	2207/I0615	6261

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WASHINGTON, DC 20005

EXAMINER
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CHEN, TSE W

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/749,792

Applicant(s)

CAI, ZHONG-NING (GEORGE)

Examiner

Tse Chen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated February 14, 2005.
2. Claims 1-20 are presented for examination.

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

#### ***Re Claims 1-4, 6-9, 11-17***

4. Claims 1-4, 6-9, 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou et al, U.S. Patent 5940785, hereinafter referred to as Georgiou, in view of McDermott et al., U.S. Patent 5233314, hereinafter referred to as McDermott.

5. In re claim 1, Georgiou disclose an apparatus for dynamic power control of a processor based on a thermal condition [abstract], comprising:

- A sensor to measure a thermal characteristic of a processor with a clock frequency [119, fig.1].
- A circuit to reduce the clock frequency of the processor [col.3, ll.60-64, col.4, ll.35-37, 48-50] responsive to the measured thermal characteristic satisfying a predetermined threshold [col.4, ll.26-33], the circuit including an input [270; rate of temperature change] to determine a temperature-related frequency reduction [col.4, ll.26-50].

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6. Georgiou did not disclose expressly a performance demanding level input to determine a *rate* of the frequency reduction.

7. McDermott taught an apparatus [fig.1] for dynamic power control of a processor [cpu 4] [col.1, l.13 – col.3, l.23] comprising:

- A circuit [clock generator 10] to reduce the clock frequency of the processor, the circuit including a performance demanding level input [lv11, 2] to determine a rate of the frequency reduction [col.4, l.66 – col.5, l.24; col.6, ll.51-64; col.8, l.45 – col.9, l.13].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Georgiou and McDermott before him at the time the invention was made, to modify *the circuit that includes an input to determine a temperature-related frequency reduction* as taught by Georgiou to include the teachings regarding *controlling frequency reductions via a rate* as taught by McDermott, in order to obtain the apparatus for dynamic power control of a processor based on a thermal condition, comprising a circuit to reduce the clock frequency of the processor responsive to the measured thermal characteristic satisfying a pre-determined threshold, *the circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction*. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better control frequency changes [McDermott: col.2, l.65 – col.3, l.23].

9. As per claim 2, Georgiou taught the thermal characteristic which includes temperature and rate of temperature change [col. 4, lines 26 – 33].

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10. As per claim 3, Georgiou taught a frequency generator and a logic circuit [fig. 4, col. 8, line 42 – 66].
11. As per claim 4, Georgiou reduces the clock frequency by less than fifty percent [col. 8, lines 48 – 49].
12. As per claim 6, Georgiou would slow down the processor when it runs too hot thereby allowing the processor, inherently, to run at a higher operating temperature.
13. As per claims 7 – 9 and 11, Georgiou and McDermott taught each and every limitation as discussed above in reference to claims 1-4 and 6. Therefore, Georgiou and McDermott taught the method in operating the apparatus.
14. In re claim 12, Georgiou and McDermott disclose each and every limitation as discussed above in reference to claim 1. Georgiou further taught the steps of:
- Entering a first state [normal operating state with normal clock frequency] from a second state [overheat state] in response to a measured thermal characteristic of a processor with a clock frequency failing to satisfy a first predetermined threshold [threshold temperature 230 which indicates the processor is overheating]<sup>1</sup> ;
  - Remaining in the first state in response to a measured thermal characteristic of the processor failing to satisfy the first pre-determined threshold [the processor remain in the normal operating state when its temperature fails to rise above the threshold temperature]; and

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<sup>1</sup> After the processor enters into a overheating state, the processor's clock frequency will be reduced until the processor is cooling off. Thereafter, the processor returns to its normal operating state, col. 9, lines 22 - 25.

- Entering the second state from the first state in response to a measured thermal characteristic of the processor satisfying the first predetermined threshold, and in the second state, performing frequency reduction [the processor enters the overheating state when the heat sensor indicates the temperature is above the threshold temperature and reduces clock frequency to reduce temperature].
15. As per claims 13 – 17, Georgiou taught the usage of temperature and rate of temperature change of the predetermined thresholds [col.4, ll.30–34].

*Re Claims 5 and 10*

16. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou and McDermott as applied to claims 1 and 7 above, and further in view of Ko, U.S. Patent 6192479.
17. Georgious and McDermott disclose each and every limitation of the claim as discussed above in reference to claims 1 and 7. Georgiou and McDermott did not discuss the details of reducing the clock frequency.
18. Ko taught an invention for power management of a processing device, the invention comprising of a circuit for reducing the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency [column 5, lines 53-58].
19. It would have been obvious to one of ordinary skill in the art, having the teachings of Georgiou, McDermott, and Ko before him at the time the invention was made, to include the teachings of Ko with the apparatus disclosed by Georgiou and McDermott as the way of reducing the clock frequency taught by Ko is a well known way suitable for reducing the clock frequency in the apparatus of Georgiou and McDermott. One of ordinary skill in the art would

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have been motivated to make such a combination as it provides a way to reduce the clock frequency and better control power conservation [Ko: col.2, ll.10-35].

*Re Claims 18-20*

20. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ko in view of Georgiou and McDermott.

21. In re claim 18, Ko discloses a processor [data processing device 21] comprising:

- Thermal sensing logic [circuit 49] to output an enabling signal taking on values responsive to whether a temperature signal meets or do not meet predetermined temperature threshold [Tok] [col.8, ll.48-53].
- Performance demanding level logic [clock arbiter 51] to output a signal [down] taking on values that permit temperature-related frequency reduction [col.6, l.32 – col.7, l.5; temperature overheat signal induces clock arbiter to issue down signal to reduce frequency].
- Frequency reduction logic coupled to the performance demanding level logic and the thermal sensing logic, to perform frequency reduction based on the values generated by the thermal sensing logic and the performance demanding level logic [col.4, ll.49-60].

22. Ko did not discuss values representing a rate of temperature change or a rate of frequency reduction.

23. Regarding the rate of temperature change, Georgiou discloses a thermal sensing logic [119, 130] to output function signals taking on values representing a function of a temperature [relative to a prior sample] and a rate of temperature change [col.4, ll.17-50; col.7, ll.12-50].

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24. It would have been obvious to one of ordinary skill in the art, having the teachings of Ko and Georgiou before him at the time the invention was made, to modify the processor taught by Ko to include the thermal sensing logic outputs taught by Georgiou, in order to obtain the processor comprising thermal sensing logic to output function signals taking on values representing a function of a temperature and a rate of temperature change, and an enabling signal taking on values responsive to whether the function signals meets or do not meet predetermined temperature and rate of temperature change thresholds. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for better clock control for power conservation [Ko: col.2, ll.10-35; Georgiou: col.3, ll.17-46].

25. Regarding the rate of frequency reduction, McDermott discloses a performance demanding logic [14] to output a signal [lv11, 2] taking on values [high, low] that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second [col.4, l.66 – col.5, l.24; col.6, ll.51-64; col.8, l.45 – col.9, l.13].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Ko and McDermott before him at the time the invention was made, to modify the processor taught by Ko to include the performance demanding logic output taught by McDermott, in order to obtain the processor comprising a performance demanding logic to output a signal taking on values that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better control frequency changes [McDermott: col.2, l.65 – col.3, l.23].



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27. As to claim 19, Georgiou discloses each and every limitation as discussed above in reference to claims 12-17.

28. As to claim 20, Ko discloses the processor wherein values output by the performance demanding level logic are responsive to a processor application [col.6, l.32 – col.7, l.5; down signal are responsive to functional unit activity status signal].

### ***Response to Arguments***

29. Applicant's arguments with respect to claims 1, 7, 12, and 18 have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

### ***Conclusion***

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen  
March 15, 2005

  
**LYNNE H. BROWNE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**